SONY

CXB1581Q

Fibre Channel Transmitter

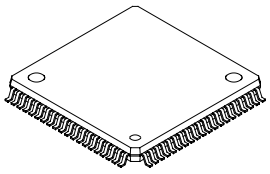
Description

The CXB1581Q is a transmitter IC with a built-in PLL for high-speed serial data transmission. It can be used together with the receiver IC CXB1582Q as a chip set, and 1062.5Mbaud, 20-bit or 531.25Mbaud, 10-bit operation can be selected.

Features

- Conforms to ANSI X3T11 Fibre channel standard
- Supports GLM (Gigabaud Link Module) interface
- Built-in PLL for synthesizing a low-jitter clock
- Single 3.3V power supply or dual 3.3V/5V power supply (for 5V TTL interface) operation can be selected.
- Low power consumption: 830mW (Typ.) when operating with a single 3.3V power supply
- 1062.5Mbaud, 20-bit or 531.25Mbaud, 10-bit operation can be selected.
- Test pattern (±K28.5) generation circuit

80 pin QFP (Plastic)



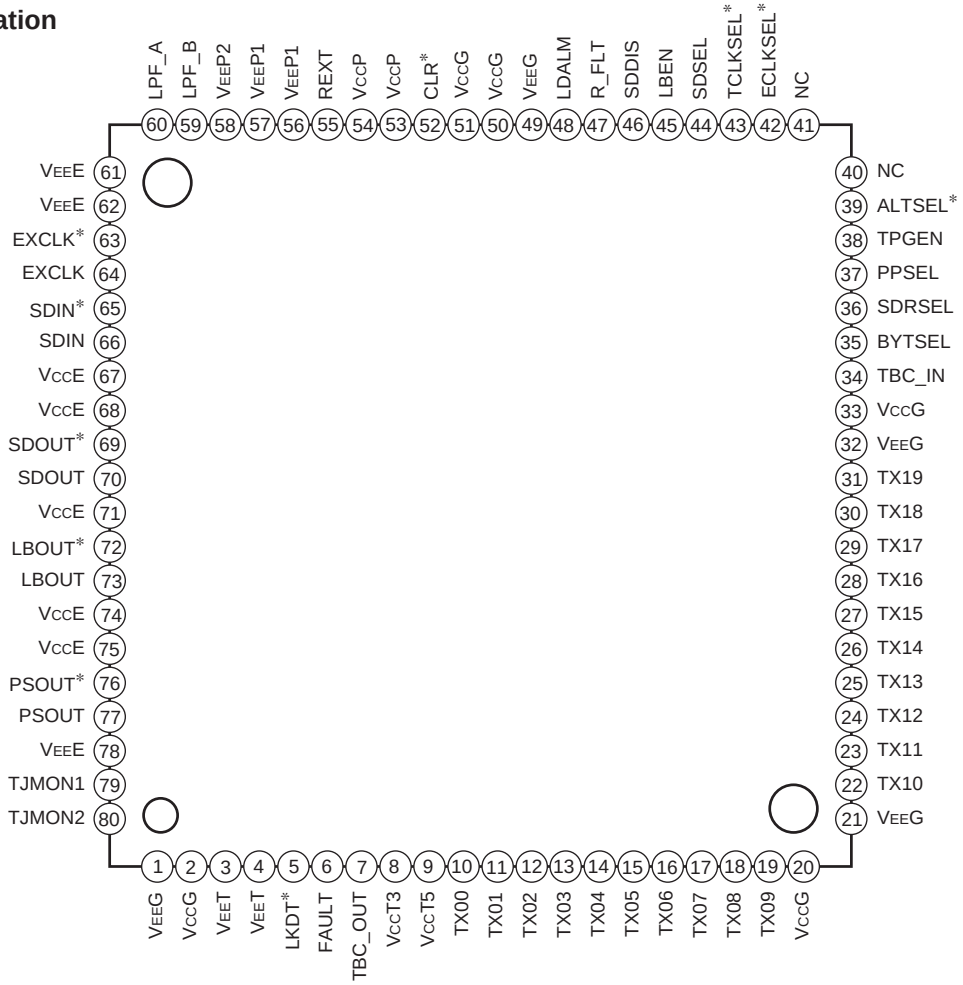
Applications

Fibre channel 1062.5Mbaud and 531.25Mbaud communications

Structure

Bipolar silicon monolithic IC

Pin Configuration



E95912A64-ST

Absolute Maximum Ratings ($V_{EE}E$, $V_{EE}T$, $V_{EE}G$, $V_{EE}P$ = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (excluding $V_{CC}T5$)	V_{CC}	–0.3		4	V
Supply voltage for TTL output	$V_{CC}T5$	$V_{CC}G$ – 2, or –0.3		$V_{CC}G$ + 5, or 5.5	V
TTL DC input voltage	V_I_T	–0.5		5.5	V
ECL DC input voltage	V_I_E	V_{CC} – 2		V_{CC}	V
ECL differential input voltage	V_{IS}_E	–2		2	V
TTL output current (High level)	I_{OH}_T	–20		0	mA
TTL output current (Low level)	I_{OL}_T	0		20	mA
ECL output current	I_O_E	–30		0	mA
Operating ambient temperature	Ta	–55		70	°C
Storage temperature	Tstg	–65		150	°C

Recommended Operating Conditions ($V_{EE}E$, $V_{EE}T$, $V_{EE}G$, $V_{EE}P$ = 0V)

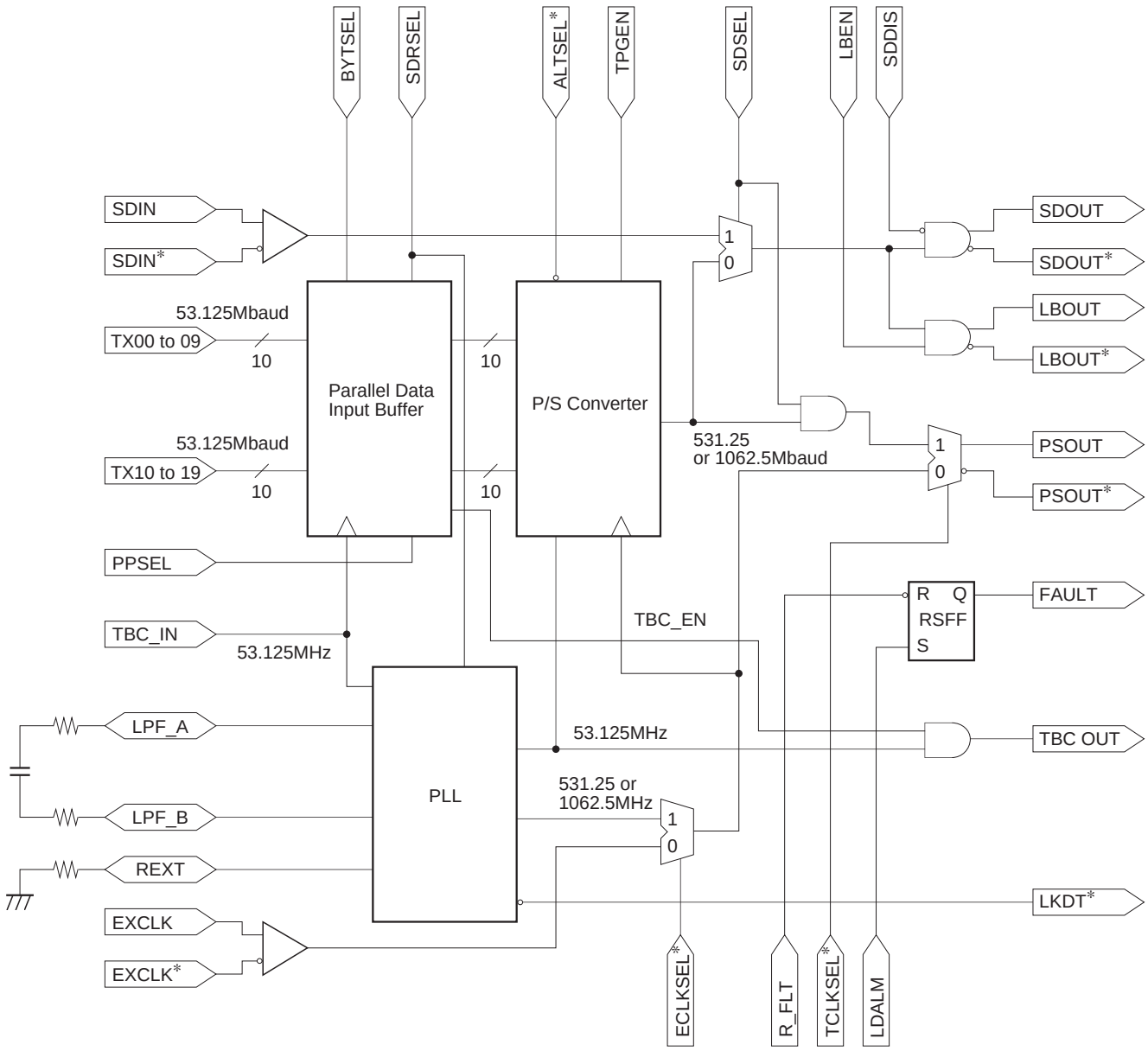
During single 3.3V power supply operation

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (including $V_{CC}T5$)	V_{CC}	3.135	3.3	3.465	V
Ambient temperature	Ta	0		70	°C

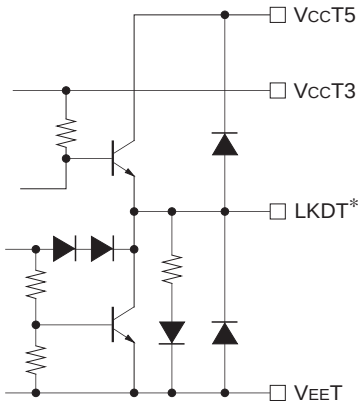
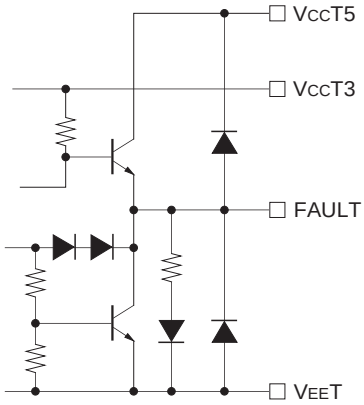
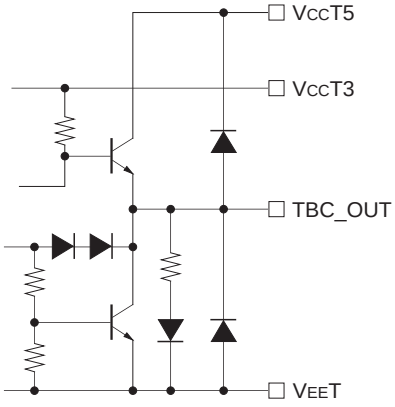
During dual 3.3V/5V power supply operation ($V_{CC}T3$ open)

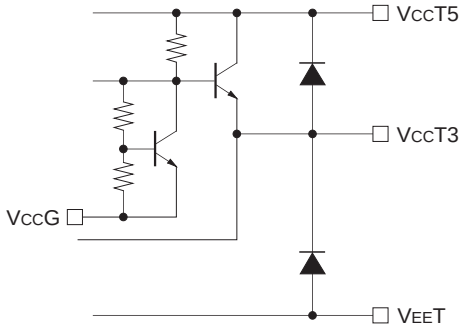
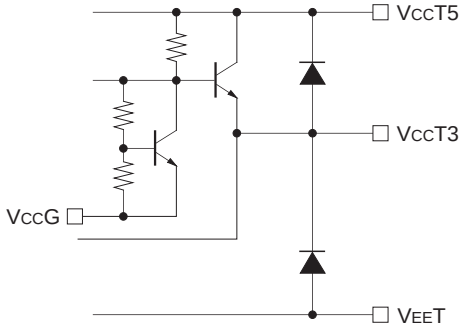
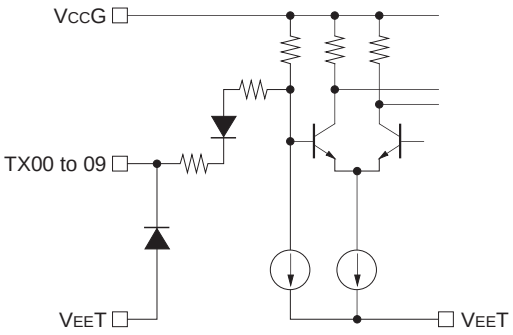
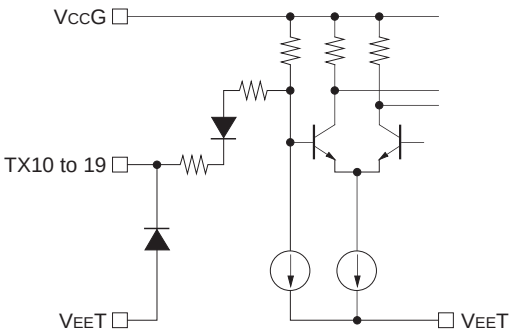
Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (excluding $V_{CC}T5$)	V_{CC}	3.135	3.3	3.465	V
Power supply for TTL output	$V_{CC}T5$	4.75	5	5.25	V
Ambient temperature	Ta	0		70	°C

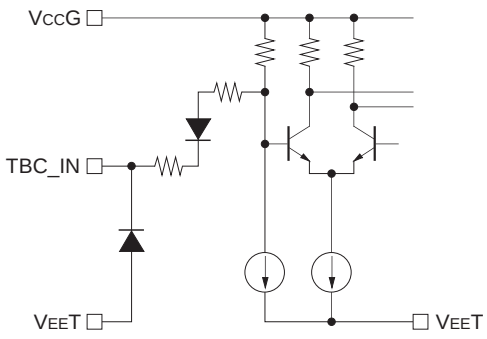
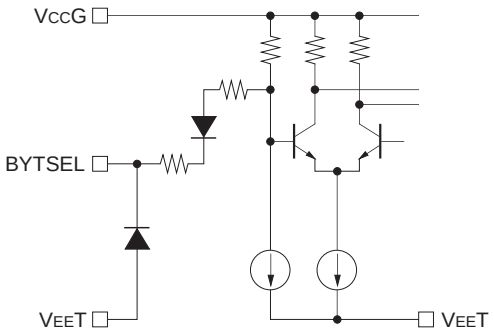
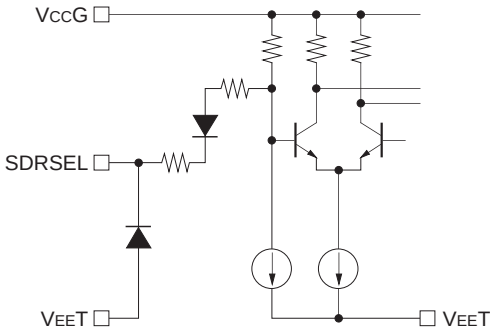
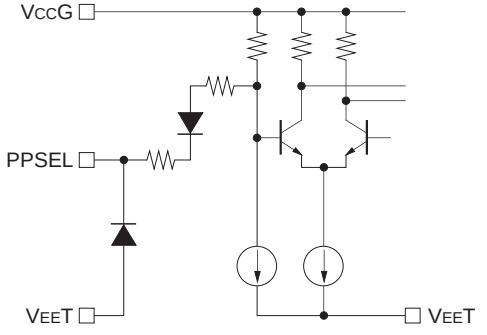
Block Diagram

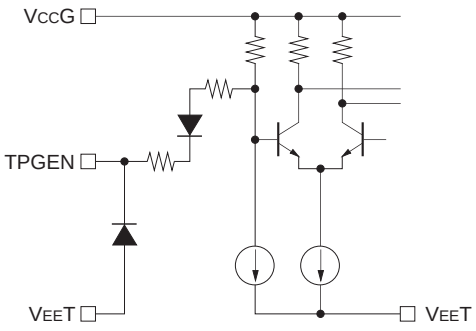
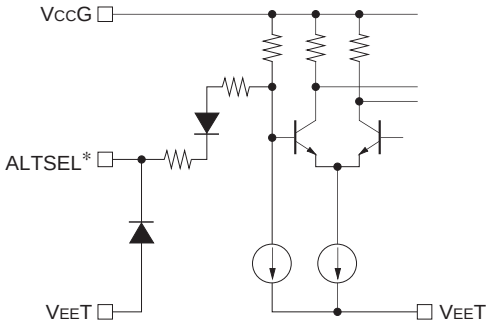
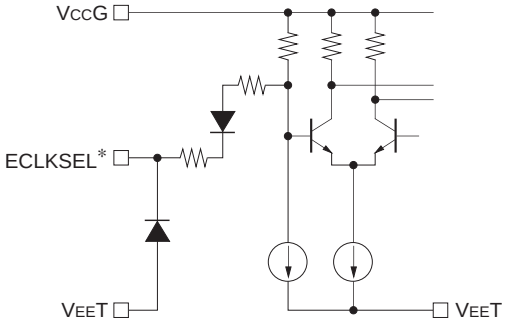
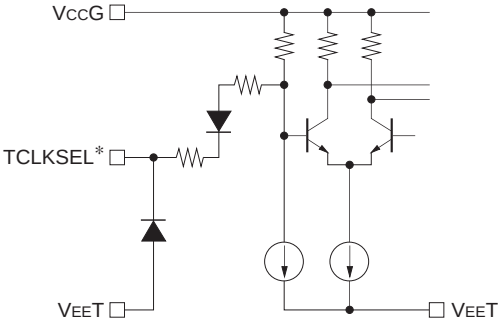


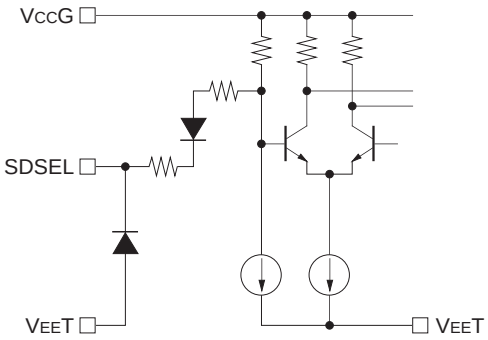
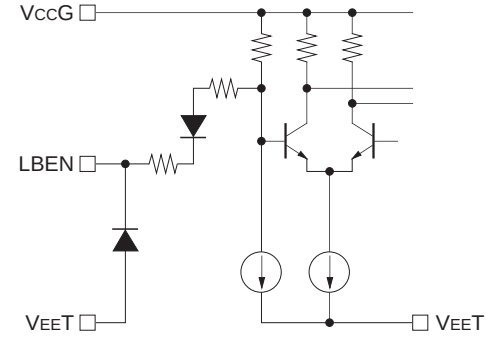
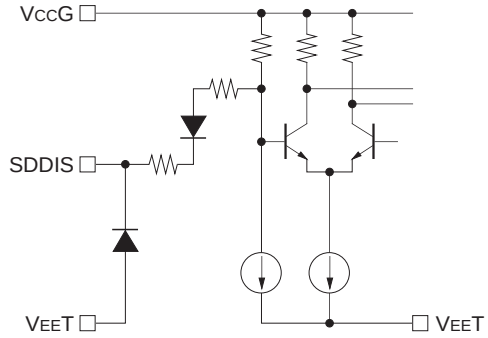
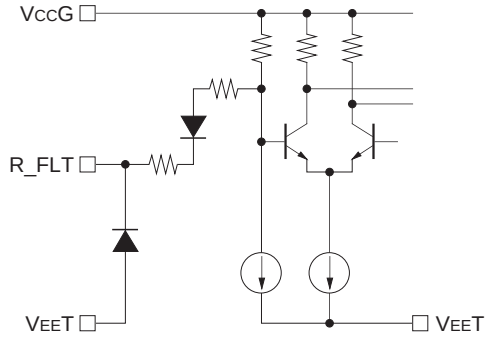
Pin Description

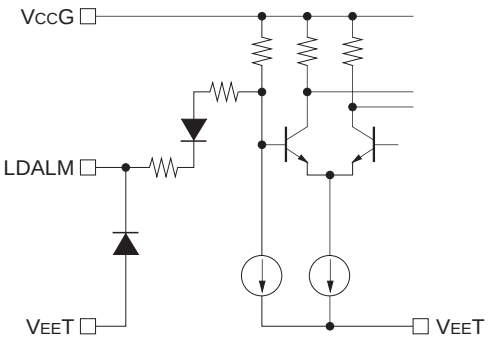
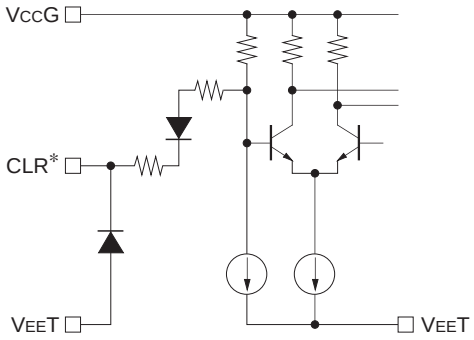
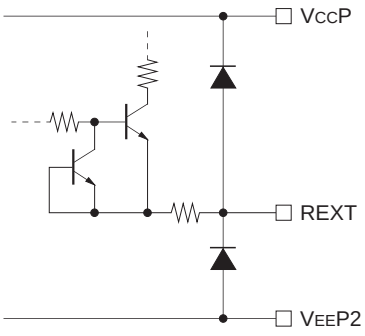
Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
1, 21, 32, 49	$V_{EE}G$	Power supply	0V	—	Negative power supplies for internal logic gate.
2, 20, 33,50, 51	$V_{CC}G$	Power supply	3.3V	—	Positive power supplies for internal logic gate.
3, 4	$V_{EE}T$	Power supply	0V	—	Negative power supplies for TTL output.
5	LKDT*	TTL output	TTL level		PLL lock detection signal output. This pin outputs low level when the PLL is locked to TBC_IN and operating normally, and high level when the PLL is not operating normally.
6	FAULT	TTL output	TTL level		FAULT signal output. This pin is used for the FAULT signal in the GLM standard. This pin outputs high level at the rising edge of LDALM and low level at the falling edge of R_RLT. (See Table 3.)
7	TBC_OUT	TTL output	TTL level		Transmission byte clock output (53.125MHz). This clock is generated by frequency-dividing the transmission bit clock (1.0625GHz or 531.25MHz).

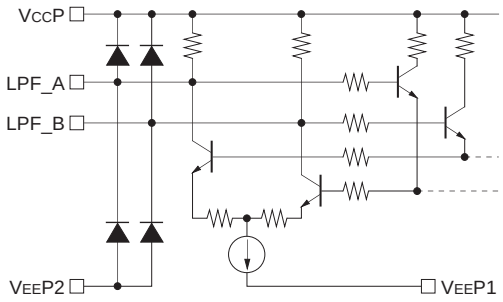
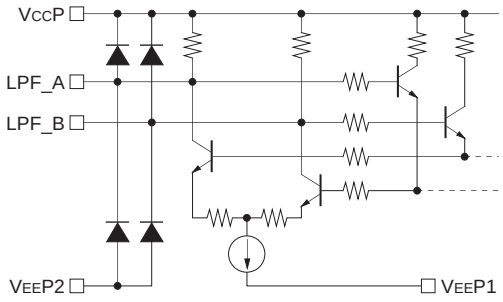
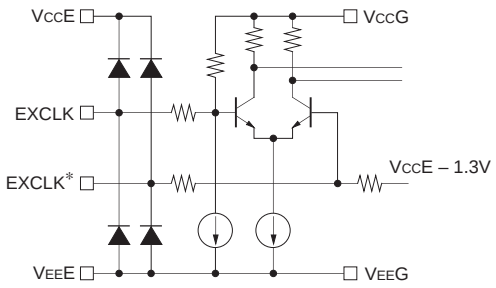
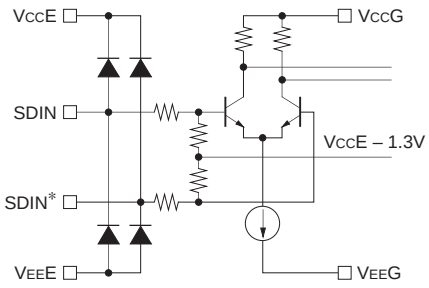
Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
8	$V_{CC}T3$	Power supply	3.3V or open		Positive power supply for TTL output. Set to 3.3V when using the IC with a single 3.3V power supply; leave open when using the IC with a dual 3.3V/5V power supply.
9	$V_{CC}T5$	Power supply	3.3V or 5V		Positive power supply for TTL output. Set to 3.3V when using the IC with a single 3.3V power supply; to 5V when using the IC with a dual 3.3V/5V power supply.
10 to 19	TX00 to 09	TTL input	TTL level		Parallel data inputs (Byte_0).
22 to 31	TX10 to 19	TTL input	TTL level		Parallel data inputs (Byte_1).

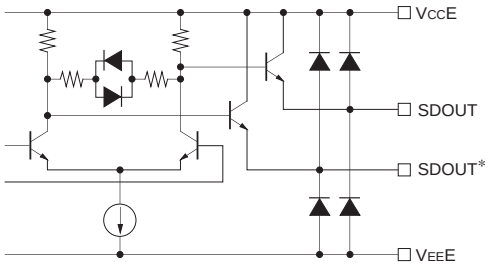
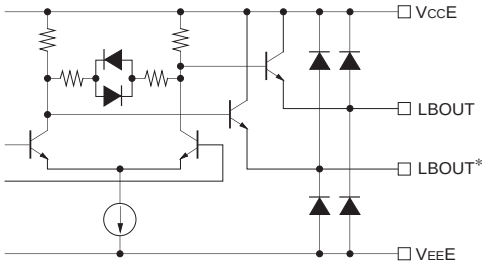
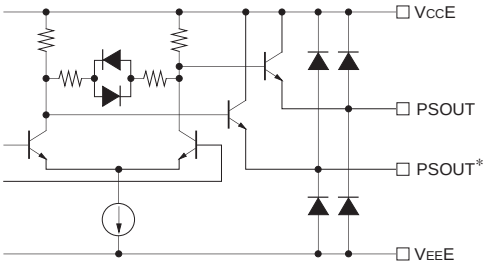
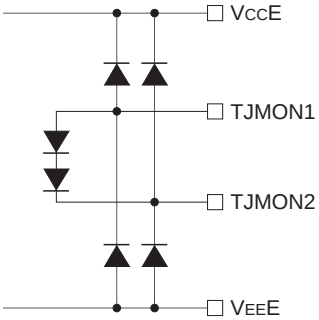
Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
34	TBC_IN	TTL input	TTL level		Transmission byte clock input (53.125MHz).
35	BYTSEL	TTL input	TTL level		Byte selection. (See Table 2.)
36	SDRSEL	TTL input	TTL level		Serial data transmission rate selection. Setting this pin to low level selects 531.25Mbaud mode and to high level selects 1.0625Gbaud mode.
37	PPSEL	TTL input	TTL level		Ping-Pong mode selection. (See Table 2 and the Timing Charts.)

Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
38	TPGEN	TTL input	TTL level		Test pattern generation control. Inputting high level to this pin generates positive or alternating disparity K28.5 (one of the 8B10B conversion codes) as the serial transfer data.
39	ALTSEL*	TTL input	TTL level		Alternating disparity selection. The test pattern generated when TPGEN is set to high level becomes alternating disparity K28.5 if this pin is set to low level, and positive disparity K28.5 if this pin is set to high level.
40, 41	NC		Open		No connection.
42	ECLKSEL*	TTL input	TTL high level or 3.3V		External clock selection. When this pin is set to low level, the clock input to EXCLK is used as the transmission bit clock.
43	TCLKSEL*	TTL input	TTL high level or 3.3V		Transmission bit clock output selection. When this pin is set to low level, the transmission bit clock is output from PSOUT. (See Table 1.)

Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
44	SDSEL	TTL input	TTL level		SDIN selection. When this pin is set to high level, the data input to SDIN is output unmodified from SDOUT.
45	LBEN	TTL input	TTL level		Loop-back enable. When this pin is set to high level, LBOUT functions as the serial data output. (See Table 1.)
46	SDDIS	TTL input	TTL level		SDOUT disable. Setting this pin to high level fixes SDOUT to low level and SDOUT* to high level. (See Table 1.)
47	R_FLT	TTL input	TTL level		Reset FAULT. FAULT output goes to low level at the falling edge of this signal. (See Table 3.)

Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
48	LDALM	TTL input	TTL lebel		Laser diode alarm signal input. FAULT output goes to high level at the rising edge of this signal. (See Table 3.)
52	CLR*	TTL input	TTL high level or 3.3V		Internal counter clear. Setting this signal to low level clears the internal counter.
53, 54	VCCP	Power supply	3.3V	—	Positive power supplies for internal PLL.
55	REXT	External part connection pin	—		Connects the resistor which determines the VCO center frequency. Connect a 4.7kΩ resistor between this pin and VEEP1. (See Notes on Operation and Fig. 1.)
56, 57	VEEP1	Power supply	0V	—	Negative power supplies for internal PLL.
58	VEEP2	Power supply	0V	—	Negative power supply for internal PLL.

Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
59	LPF_A	External part connection pin	—		External loop filter connection. (See Notes on Operation and Fig. 1.)
60	LPF_B	External part connection pin	—		External loop filter connection. (See Notes on Operation and Fig. 1.)
61, 62, 78	VEEE	Power supply	0V	—	Negative power supplies for ECL I/O.
64 63	EXCLK EXCLK*	ECL input (differen -tial)	Open		External clock inputs. When ECLKSEL* is set to low level, the clock input to these pins is used as the transmission bit clock. EXCLK is biased to become low level when left open.
66 65	SDIN SDIN*	ECL input (differen -tial)	ECL level		Serial data inputs. When SDSEL is set to high level, the data input to these pins is output unmodified from SDOUT.

Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
67, 68, 71, 74, 75	$V_{CC}E$	Power supply	3.3V	—	Positive power supplies for ECL I/O.
70 69	SDOUT SDOUT*	ECL output (differen -tial)	ECL level		Serial data outputs for transmission. The serial data order is TX00 → TX19 for 1GHz mode and TX00 → TX09 (Byte_0) or TX10 → TX19 (Byte_1) for 531MHz mode.
73 72	LBOUT LBOUT*	ECL output (differen -tial)	ECL level		Serial data outputs for loop-back test.
77 76	PSOUT PSOUT*	ECL output (differen -tial)	ECL level		Parallel/serial conversion outputs. These outputs are enabled when SDSEL is high level. (See Table 1.)
79 80	TJMON1 TJMON2	Test pin	Open		Junction temperature measurement.

Description of Operation Tables

TCLKSEL*	SDSEL	LBEN	SDDIS	SDOUT	LBOUT	PSOUT
L	L	L	L	Serialized Data	Fixed to Low	Trans. Bit Clock
L	L	L	H	Fixed to Low	Fixed to Low	Trans. Bit Clock
L	L	H	L	Serialized Data	Serialized Data	Trans. Bit Clock
L	L	H	H	Fixed to Low	Serialized Data	Trans. Bit Clock
L	H	L	L	SDIN	Fixed to Low	Trans. Bit Clock
L	H	L	H	Fixed to Low	Fixed to Low	Trans. Bit Clock
L	H	H	L	SDIN	SDIN	Trans. Bit Clock
L	H	H	H	Fixed to Low	SDIN	Trans. Bit Clock
H	L	L	L	Serialized Data	Fixed to Low	Fixed to Low
H	L	L	H	Fixed to Low	Fixed to Low	Fixed to Low
H	L	H	L	Serialized Data	Serialized Data	Fixed to Low
H	L	H	H	Fixed to Low	Serialized Data	Fixed to Low
H	H	L	L	SDIN	Fixed to Low	Serialized Data
H	H	L	H	Fixed to Low	Fixed to Low	Serialized Data
H	H	H	L	SDIN	SDIN	Serialized Data
H	H	H	H	Fixed to Low	SDIN	Serialized Data

Table 1. ECL Output Selection Table

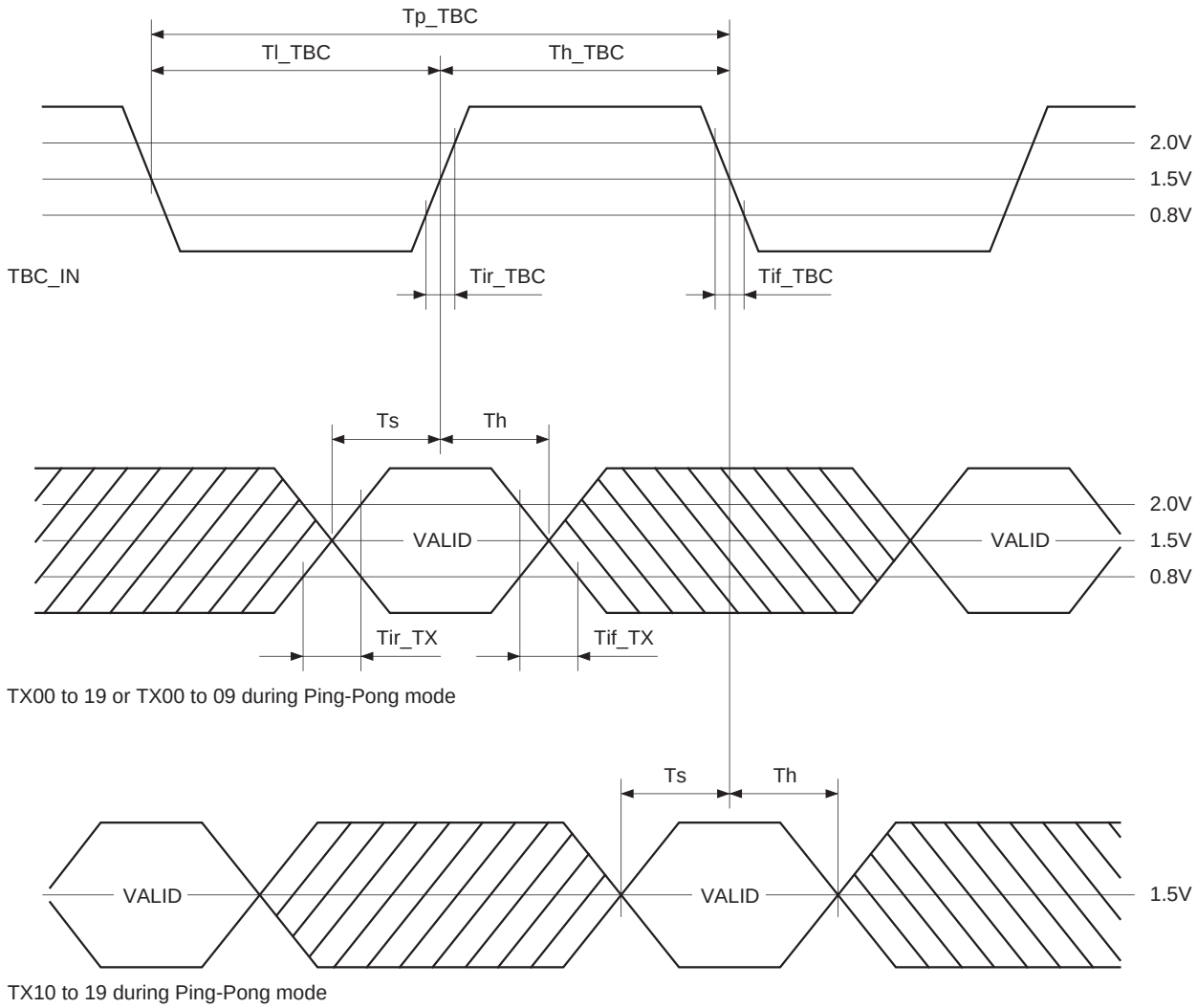
SDRSEL	BYTSEL	PPSEL	Operation mode	TBC_OUT
L	L	L	531Mbaud, Byte0 selected	Trans. Byte Clock
L	L	H	531Mbaud, Byte0 selected	Fixed to Low
L	H	L	531Mbaud, Byte1 selected	Trans. Byte Clock
L	H	H	531Mbaud, Byte1 selected	Fixed to Low
H	L	L	1062.5Mbaud, Ping-Pong OFF	Trans. Byte Clock
H	L	H	1062.5Mbaud, Ping-Pong ON	Trans. Byte Clock
H	H	L	1062.5Mbaud, Ping-Pong OFF	Fixed to Low
H	H	H	1062.5Mbaud, Ping-Pong ON	Fixed to Low

Table 2. Operation Mode Selection Table

LDALM	R_FLT	FAULT
L	H → L	L
L → H	L	H
H → L	L	H
L	L → H	H
L	H → L	L
L → H	L	H
H	L → H	H
H	H → L	L

Table 3. FAULT Function Table

Timing Charts



Electrical Characteristics

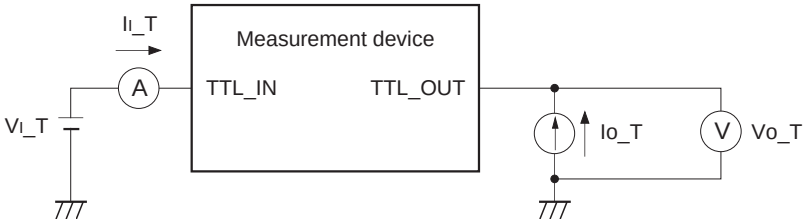
DC Characteristics (under the recommended operating conditions)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
TTL high level input voltage	aV_{IH}_T	2		5.5	V	
TTL low level input voltage	V_{IL}_T	0		0.8	V	
TTL high level input current	I_{IH}_T			20	µA	$V_{IH} = V_{CC}$
TTL low level input current	I_{IL}_T	–400			µA	$V_{IL} = 0$
TTL high level output voltage	V_{OH}-T					
Single 3.3V power supply		2.2			V	I_{OH} = –0.4mA
Dual 3.3V/5V power supply		2.6			V	I_{OH} = –0.4mA
TTL low level output voltage	V_{OL}_T					
Single 3.3V power supply				0.5	V	I_{OL} = 2mA
Dual 3.3V/5V power supply				0.5	V	I_{OL} = 4mA
ECL high level input voltage	V_{IH}_E	V_{CC} – 1.17		V_{CC} – 0.88	V	
ECL low level input voltage	V_{IL}_E	V_{CC} – 1.81		V_{CC} – 1.48	V	
ECL differential input voltage	V_{IS}_E	200		1000	mV	AC coupling input
ECL high level output voltage	V_{OH}_E	V_{CC} – 1.05		V_{CC} – 0.81	V	50Ω terminated to V_{CC} – 2V
ECL low level output voltage	V_{OL}_E	V_{CC} – 1.81		V_{CC} – 1.55	V	50Ω terminated to V_{CC} – 2V
ECL output amplitude	V_{OS}_E	650			mV	50Ω terminated to V_{CC} – 2V
Current consumption	I_{CC}					Output pins open
Single 3.3V power supply			250	313	mA	
Dual 3.3V/5V power supply			237 13	297 17	mA mA	3.3V power supply 5V power supply (V_{CC}T5)
Power consumption	P_D					Output pins open
Single 3.3V power supply			0.83	1.1	W	
Dual 3.3V/5V power supply			0.85	1.12	W	

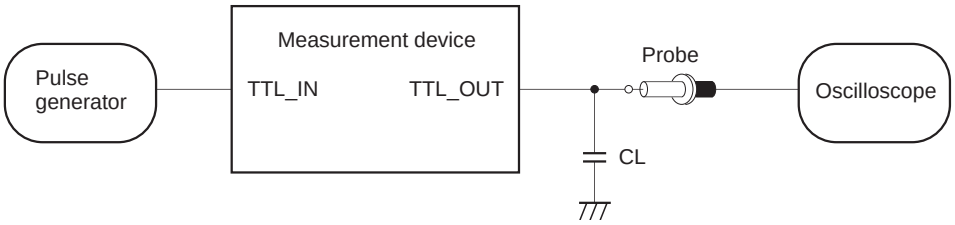
AC Characteristics (under the recommended operating conditions)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
TX00 to 19 rise time	Tir_TX			4.8	ns	0.8 to 2.0V
TX00 to 19 fall time	Tif_TX			4.8	ns	2.0 to 0.8V
TBC_IN rise time	Tir_TBC			2.4	ns	0.8 to 2.0V
TBC_IN fall time	Tif_TBC			2.4	ns	2.0 to 0.8V
TTL output rise time	Tor_T					
Single 3.3V power supply				3.5	ns	0.8 to 2.0V, CL = 10pF
Dual 3.3V/5V power supply				3.2	ns	0.6 to 2.2V, CL = 10pF
TTL output fall time	Tof_T					
Single 3.3V power supply				3.5	ns	2.0 to 0.8V, CL = 10pF
Dual 3.3V/5V power supply				3.2	ns	2.2 to 0.6V, CL = 10pF
ECL output rise time	Tor_E			400	ps	20 to 80%, CL ≤ 2pF
ECL output fall time	Tof_E			400	ps	20 to 80%, CL ≤ 2pF
TBC_IN cycle	Tp_TBC	18.2	18.8	22.2	ns	
TBC_IN low time	Tl_TBC	6			ns	
TBC IN high time	Th_TBC	6			ns	
TX setup time	Ts	1.8			ns	
TX hold time	Th	1.8			ns	
Deterministic jitter (p-p)	DJ		0.02	0.07	UI	±K28.5 serial data output
Random jitter (p-p)	RJ		0.18	0.23	UI	Serial data output

Electrical Characteristics Measurement Circuit (See Fig. 3 Power Supply Circuits regarding the power supply.)

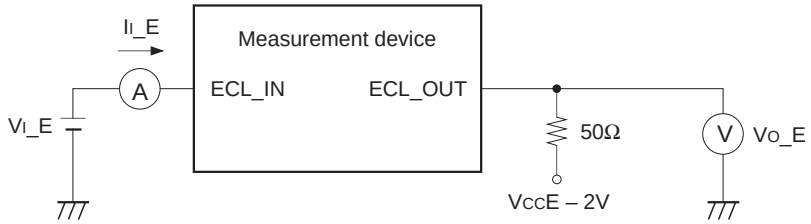


(a) TTL I/O DC characteristics measurement circuit

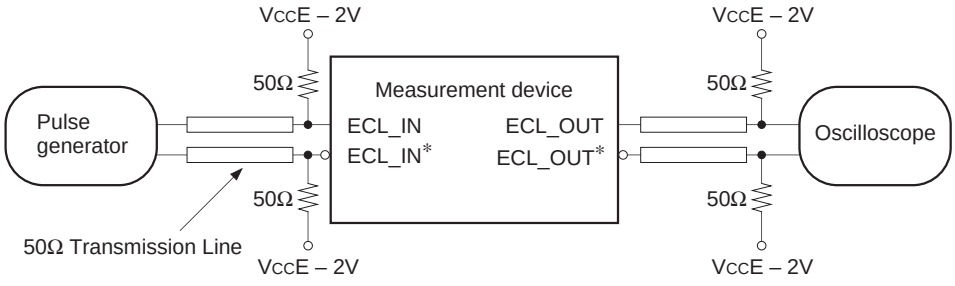


CL = 10pF (including the probe capacitance)

(b) TTL I/O AC characteristics measurement circuit

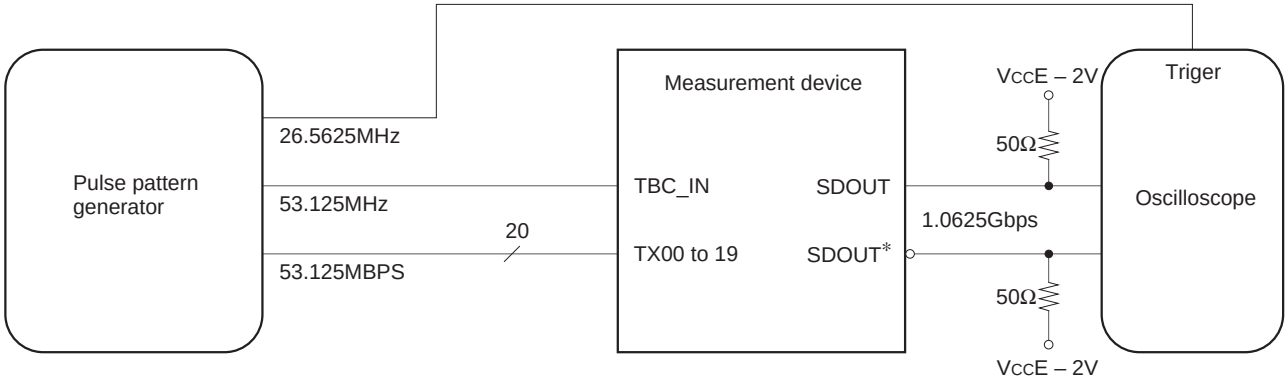


(c) ECL I/O DC characteristics measurement circuit



CL ≤ 2pF (input capacitance of the measurement instrument and floating capacitance)

(d) ECL I/O AC characteristics measurement circuit

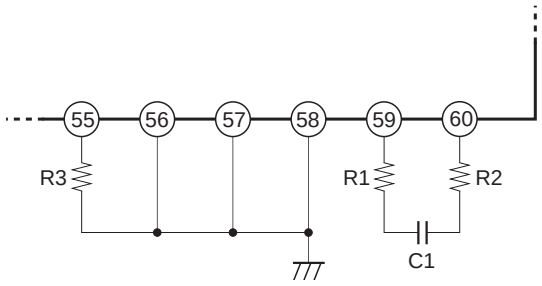


(e) Jitter characteristics measurement circuit

Notes on Operation

1. Clock synthesizer (PLL)

The CXB1581Q has a built-in PLL-based clock synthesizer for generating the serial data transmission frequency clock (transmission bit clock) from TBC_IN. This clock synthesizer requires an external loop filter and an external resistor which determines the VCO center frequency. The external part circuit and recommended constant values are shown in the figure below. The parasitic capacitance attached to the IC pins (Pins 55, 59 and 60) which are used to connect external parts should be kept as small as possible in order to obtain the good PLL characteristics. In addition, resistor R3 should have a small temperature coefficient to reduce the temperature dependence of the VCO oscillation frequency.

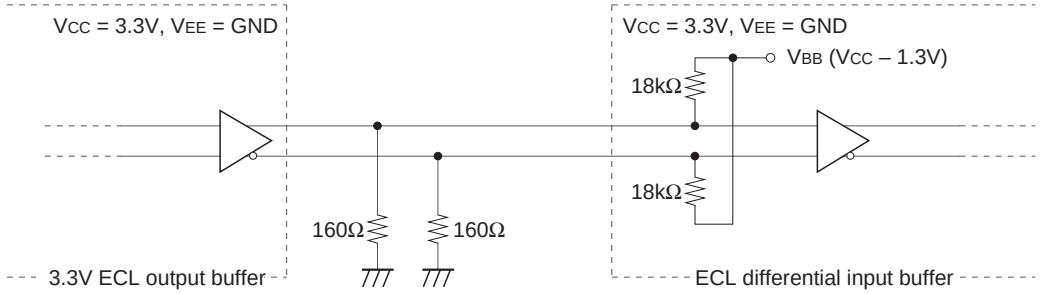


R1: 1.5kΩ
R2: 1.5kΩ
R3: 4.7kΩ
C1: 0.01µF

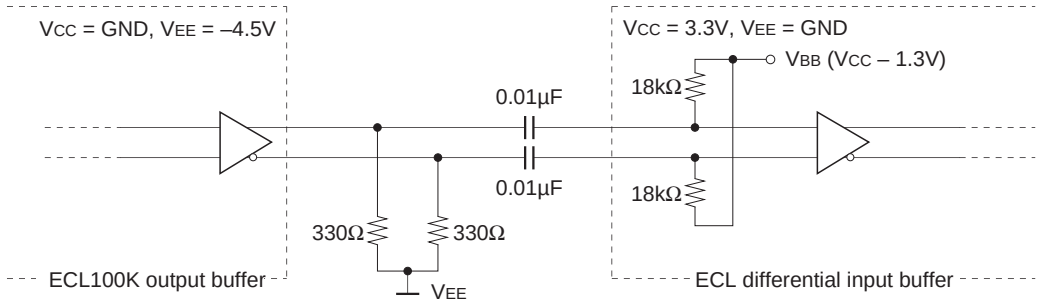
Fig. 1. External Part Circuit and Recommended Constants

2. ECL input circuit

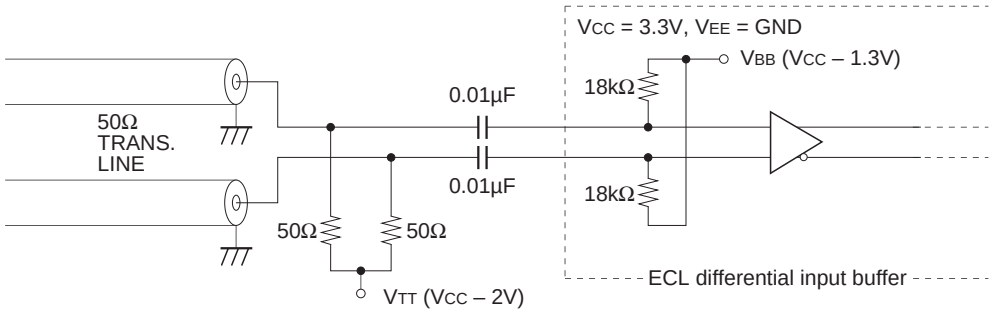
The ECL differential input pins (excluding EXCLK) of the CXB1581Q are biased to V_{BB} (V_{CC} – 1.3V) via an 18kΩ resistor in the IC. See the figures below for ECL differential input methods.



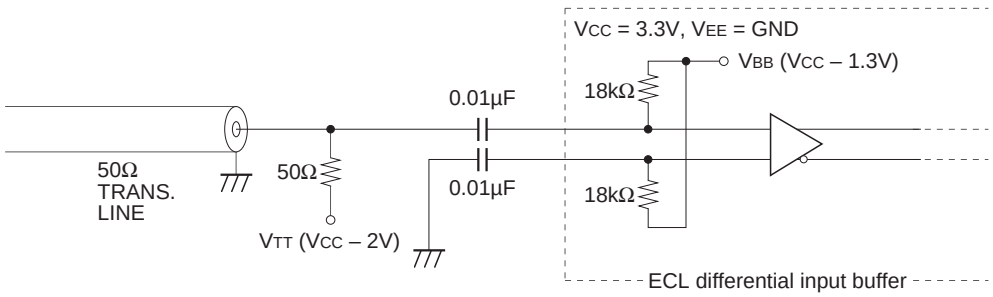
(a) ECL differential signal from 3.3V ECL output buffer



(b) ECL differential signal from ECL100K output buffer



(c) ECL differential signal from 50Ω transmission line

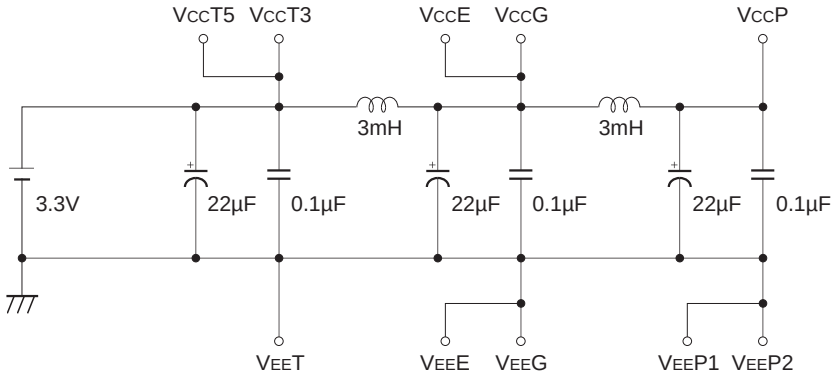


(d) ECL single signal from 50Ω transmission line

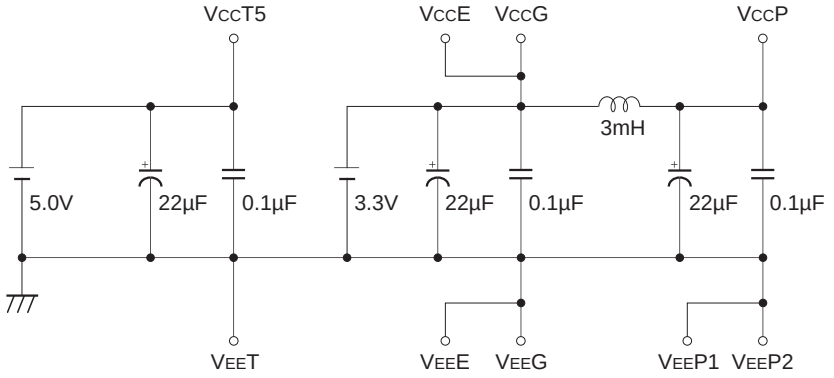
Fig. 2. ECL Input Circuits

3. Power supply

Power can be supplied to the CXB1581Q by either a single 3.3V power supply or a dual 3.3V/5V power supply. When a TTL output high level of 2.2V is sufficient (for example, when only interfacing with a 3.3V CMOS), use a single 3.3V power supply. When a TTL output high level of greater than 2.2V is required (for example, when interfacing with a 5V TTL/CMOS), use a dual 3.3V/5V power supply.



(a) Single 3.3V power supply

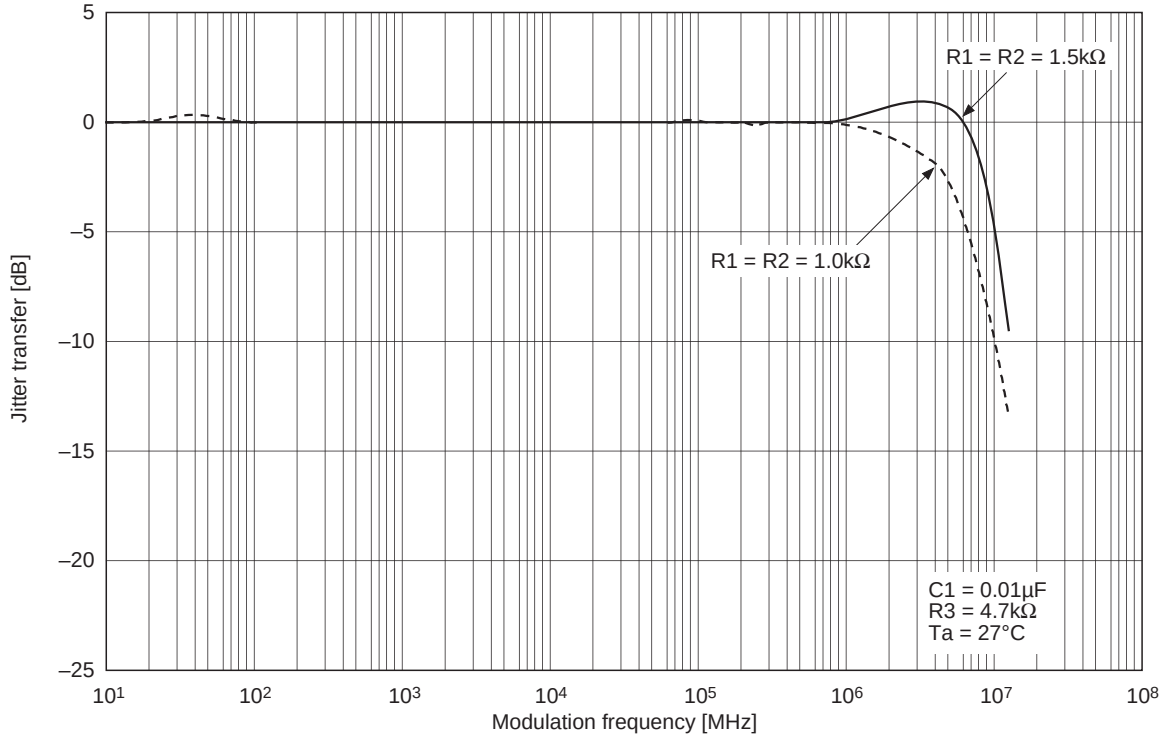


(b) Dual 3.3V/5V power supply

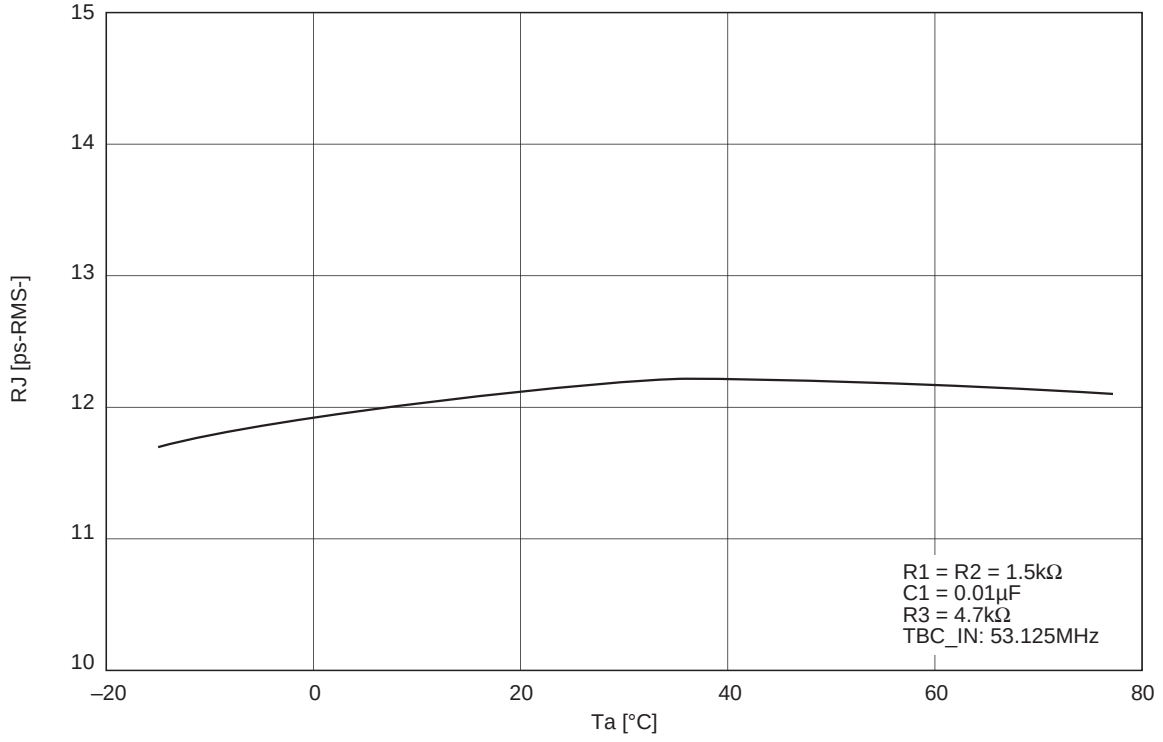
Fig. 3. Power Supply Circuits

Example of Representative Characteristics

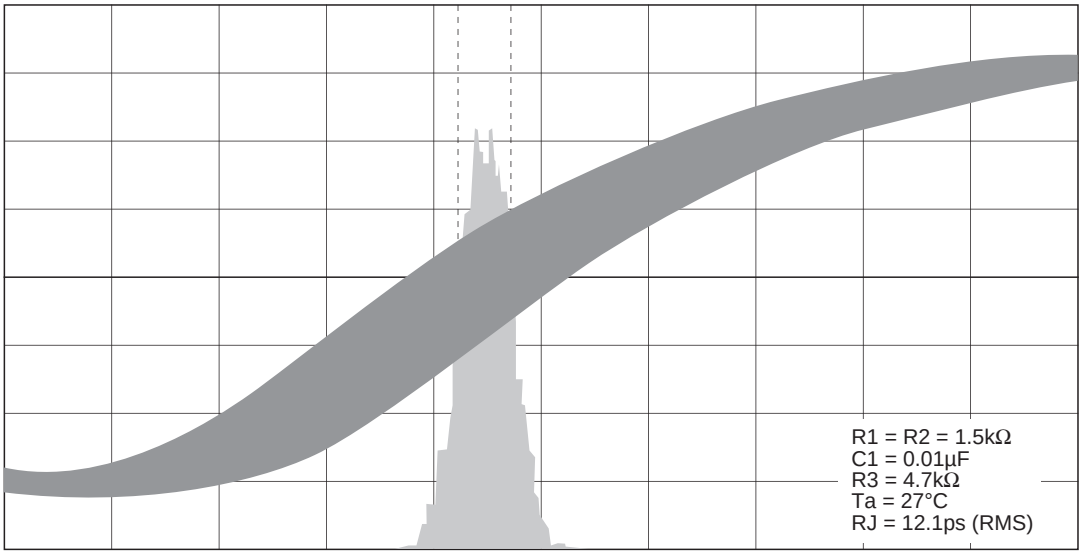
Jitter transfer (1.0625GHz operation)



RJ temperature characteristics (SDOUT, 1.0625GHz operation)

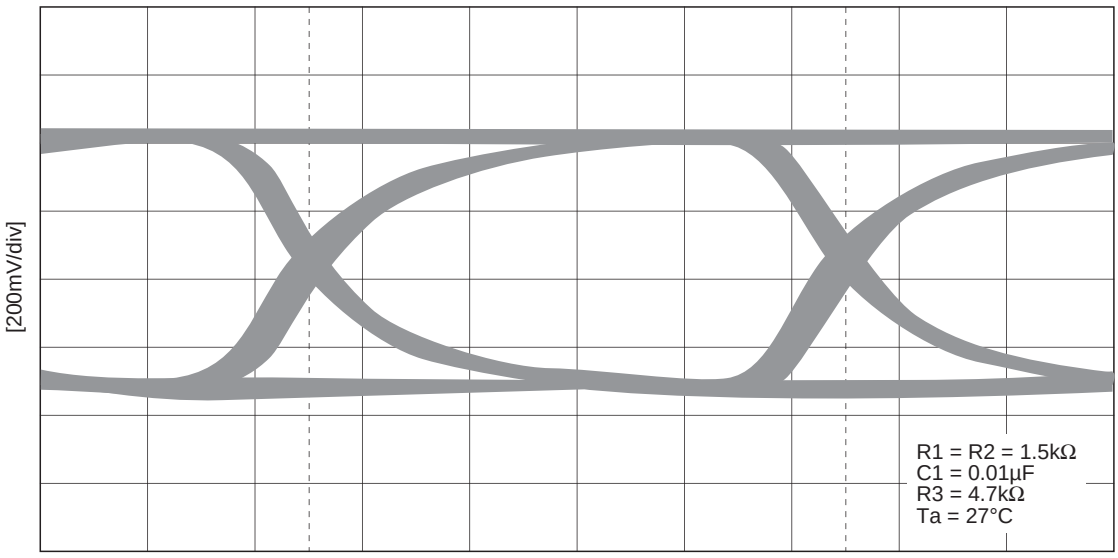


Exampe of RJ measurement (SDOUT, 1.0625GHz operation)



[50ps/div]

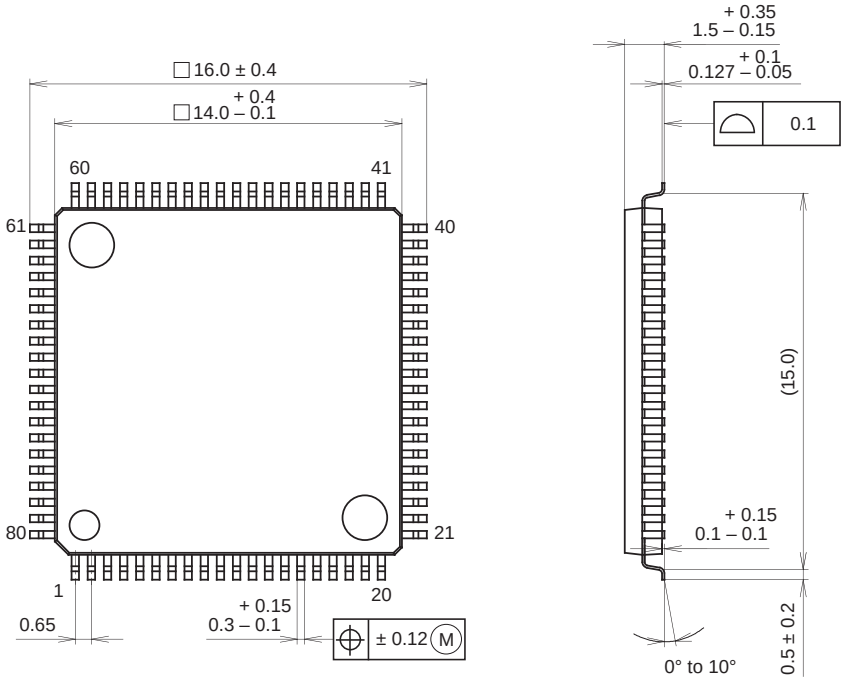
Eye pattern (SDOUT, 1.0625GHz operation)



[200ps/div]

Package Outline Unit: mm

80PIN QFP (PLASTIC)



SONY CODE	QFP-80P-L03
EIAJ CODE	LQFP080-P-1414
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.6g